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Microfabrication of 3D silicon MEMS structures using gray-scale lithography and deep reactive ion etching

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Abstract

Micromachining arbitrary 3D silicon structures for micro-electromechanical systems can be accomplished using gray-scale lithography along with dry anisotropic etching. In this study, we have investigated the use of deep reactive ion etching (DRIE) and the tailoring of etch selectivity for precise fabrication. Silicon loading, the introduction of an O_2 step, wafer electrode power, and wafer temperature are evaluated and determined to be effective for coarsely controlling etch selectivity in DRIE. The non-uniformity and surface roughness characteristics are evaluated and found to be scaled by the etch selectivity when the 3D profile is transferred into the silicon. A micro-compressor is demonstrated using gray-scale lithography and DRIE showing that etch selectivity can be successfully tailored for a specific application.

Keywords: Gray-scale lithography; DRIE; MEMS; Etch selectivity

1. Introduction

The ability to develop 3D microstructures is of great importance for increasing optical and electro-mechanical device performance. Previous technologies use multiple direct writing steps, multiple photolithography steps, or customized equipment [1–5]. These technologies, however, are restricted to a limited range of shapes, or do not utilize batch processes. Gray-scale technology has emerged enabling the development of arbitrary 3D microstructures in various materials [6–9]. Use of gray-scale technology allows 3D shaping of silicon to be performed in a single photolithography step with subsequent dry etching.

The three key steps of gray-scale technology are shown in Fig. 1: (a) gray-scale mask design, (b) gray-scale lithography and (c) dry anisotropic etching. Steps (a) and (b) yield a precisely designed 3D profile in a photoresist-masking layer by modulating the intensity incident on the photoresist surface. Step (c) allows the 3D profile in the photoresist to be transferred into the underlying silicon substrate by dry anisotropic etching. There has been much advancement in the gray-scale mask design and lithography steps in the past few years [10–14], yet focus on the third step has been limited.

Until recently, gray-scale patterning was primarily used for defining diffractive optical elements (DOEs) [6,8,9,12,15], where etch depth requirements are typically shallow and achieved using reactive ion etching (RIE) or ion milling [6,14]. In micro-electromechanical systems (MEMS), larger silicon 3D geometries with greater depths are becoming necessary for applications such as micro-compressors [16–18], where RIE or ion milling are no longer viable. Deep reactive ion etching (DRIE) is a prime candidate to extend gray-scale technology to the depths required by current MEMS applications.

Transferring gray-scale patterned photoresist into silicon by DRIE was first demonstrated and patented by Whitley et al. [19]. Previously, researchers did not use DRIE due to the possibility that inherent scalloping from cycling passivation and etching steps would cause significant surface roughness. Whitley et al. showed that a smooth transfer could be achieved by decreasing the passivation. However, key to the success of gray-scale pattern transfer by DRIE is the etch selectivity between silicon and photoresist, which was not discussed in depth by Whitley et al.

Conventionally, etch selectivity is maximized so thin photoresist-masking layers can survive deep etches while maintaining good etch characteristics such as vertical profiles, fast silicon etch rates, and smooth surfaces. Conversely, transferring gray-scale patterned features relies on etching through the variable height photoresist to define the

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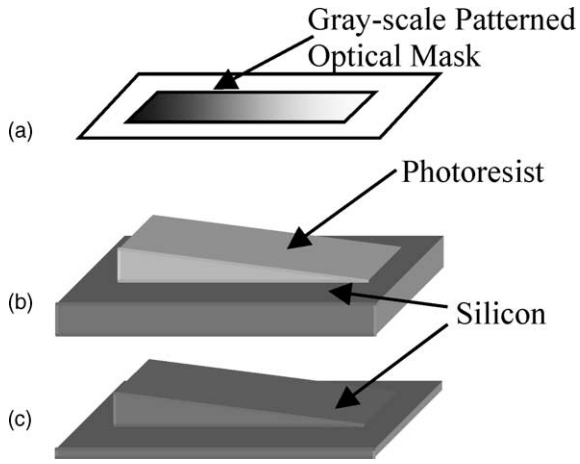

Fig. 1. The three primary steps in gray-scale technology: (a) gray-scale mask design; (b) exposure and development of the 3D pattern in photoresist; (c) transfer of photoresist structure into the silicon substrate.

silicon profile. In this case, silicon masked by thin photoresist will begin etching before the silicon masked by thicker photoresist. Therefore, the ability to control etch selectivity is necessary to precisely transfer the entire photoresist pattern to the desired depth.

This paper investigates the transfer of gray-scale patterned photoresist structures into silicon by DRIE. Effects of DRIE process parameters on etch selectivity between photoresist and silicon is evaluated. Additionally, the non-uniformity of photoresist and silicon are analyzed as well as the surface roughness of the final etched silicon surfaces. The results will serve as a guide for tailoring the etch selectivity in DRIE for developing 3D silicon structures with better precision. From these investigations, a micro-compressor is designed and demonstrated using gray-scale patterning and DRIE.

2. Experimental approach

2.1. Gray-scale mask and lithography

Gray-scale lithography utilizes an optical mask (Fig. 1a) patterned with sub-resolution pixels and spacing (pitch). This optical mask combined with projection lithography (wafer stepper) allows a uniform "DC" intensity on the photoresist surface across the pixilated region patterned using constant pitch and constant pixel sizes [10]. Changing the size of the pixels and pitches modulates the amplitude of the intensity; with each distinct intensity level termed a gray level. By this, the remaining height profile in the photoresist after development (composed of photoresist gray levels) will depend upon the incident intensity, time of exposure, and photoresist contrast (Fig. 1b). Tight processing tolerances lead to a controlled, repeatable profile in the photoresist for use as a 3D patterned masking layer [14].

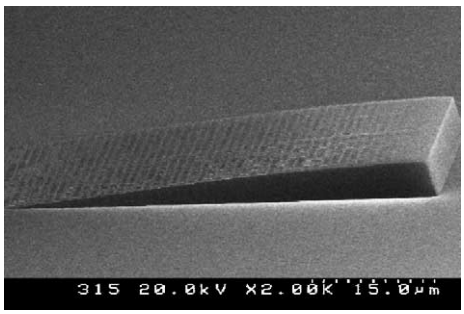

Fig. 2. Example photoresist wedge structure accomplished using gray-scale lithography. The wedge is 69 μm long and 5 μm tall.

Gray-scale optical masks were designed and developed for a GCA Ultratech wafer stepper ($\lambda = 365$ nm, resolution ~0.56 μm, and 5× reduction) to produce various wedge shaped structures in positive photoresist for characterization of the profile transfer by DRIE. An example AZ 9260 photoresist wedge structure composed of 45 different gray levels is shown in Fig. 2. The gray levels were patterned on the optical mask by varying the size of 1–2 μm sub-resolution pixels within constant sub-resolution pitches between 2 and 3 μm. Due to optical mask fabrication limitations only a finite number of gray levels exist within the chosen method of patterning, yielding a stepped profile in the photoresist. More complex patterning schemes exist realizing thousands of gray levels [6], however, for characterization purposes they are unnecessary.

Also included on the optical masks were features to measure non-uniformity in the photoresist for two gray level heights (1.6 and 1.7 μm pixels within a 2.4 μm pitch) and a conventional opaque region (no exposure). The opaque features will yield information on the uniformity of the photoresist spinning, where the gray level features include non-uniformities coming from all steps: photoresist spinning, exposure, and development steps.

2.2. DRIE experiments

DRIE pattern transfer is performed using a Unaxis, Plasma-Therm 770 ICP etcher with multiplexing capabilities. The parameters of this system used to control the etch characteristics include the input gas and flow rate, wafer electrode power, RF coil power, chamber pressure (automatic pressure control valve), temperature, and the time of etch and passivation steps. Fig. 3 shows an example DRIE etch of various sized wedge structures after a 150 μm DRIE etch with an etch selectivity of 60.

By varying system parameters, the relative etch rates of silicon and photoresist can be altered to yield recipes with a wide range of etch selectivities. AZ 9245 photoresist with a thickness of 6 μm developed in AZ 400K 1:3 DI water was used for all selectivity experiments. Wafers 75 mm in diameter and 400 μm thick were used with a silicon loading (amount of silicon exposed to the plasma) of 42%. A base

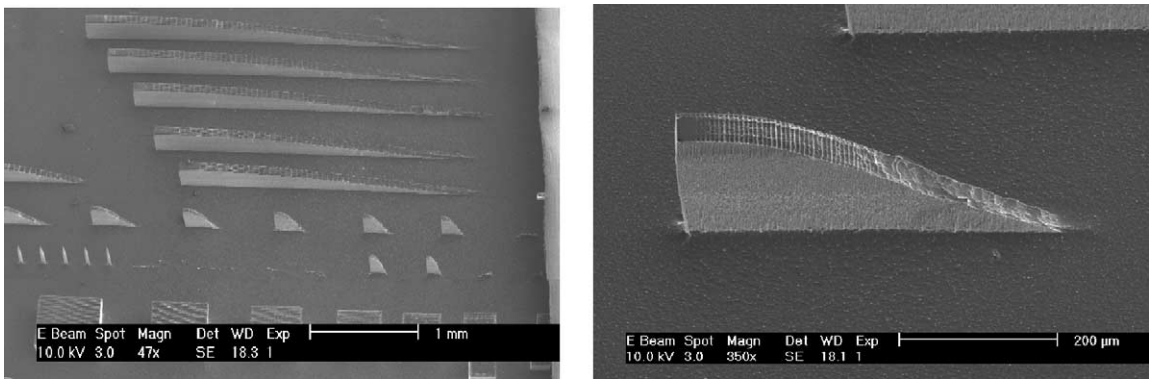

Fig. 3. Example silicon wedge structures accomplished using gray-scale lithography with the silicon etched to a depth of 150 μm by DRIE.

Table 1
DRIE base etch parameters for one passivation and etch cycle

Steps	Gas flow rates (sccm)			Chamber pressure (Pa)	Coil power (W)	Electrode power (W)	Time (s)	Cooling temperature (°C)
	SF_6	C_4F_8	Ar					
Passivation	0	70	40	2.53	825	1	5	20
Etch	100	0	40	2.53	825	10	8	20

etch recipe (Table 1) was used with a set number of 100 cycles as a reference when comparing the results of parameter variation.

Gray level structures, 500 μm × 500 μm and 50 μm × 50 μm, were used to determine the effect of each system parameter on etch selectivity, sidewall profile, and etch rate. The etch selectivity was measured as the ratio of the gray level height in silicon (full removal of the photoresist gray level) divided by the original gray level height in photoresist. Five measurements were taken on five different dies across the wafer giving 25 measurements per wafer.

The structure shown in Fig. 4 was then viewed by scanning electron microscopy (SEM) to obtain the angle of the sidewall profiles. Both the inside at the top (I_{Top}) and bottom (I_{Bottom}) were measured along with the total height of the etched structure (D_{Si}). The angle of the inside sidewall is calculated by

$$\text{Inside angle} = \tan^{-1}\left[\left(\frac{(I_{Top} - I_{Bottom})/2}{D_{Si}}\right)\right]. \quad (1)$$

The outside sidewall angles of the structures is calculated by

$$\text{Outside angle} = \tan^{-1}\left[\left(\frac{(O_{Top} - O_{Bottom})/2}{D_{Si}}\right)\right], \quad (2)$$

where O_{Top} and O_{Bottom} are measures of the top width and bottom width of the outside portions of the structure, respectively. The angles obtained will be negative for a re-entrant profile and positive for a positive profile.

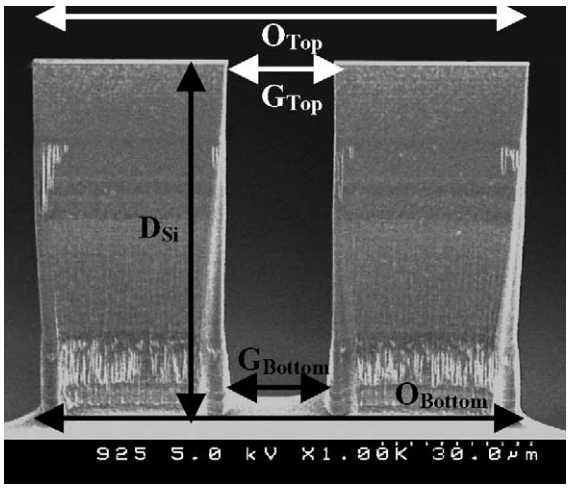

Fig. 4. SEM showing the structures used to measure the inside sidewall angle and outside sidewall angle.

The etch selectivity resulting from the base etch recipe shown in Table 1 was 75, typical when compared to standard planar etch recipes. The etch rate was 0.71 μm/cycle giving a total etch depth of 71 μm. The gap profile was re-entrant with an angle of −0.12°, and the outside profile, also re-entrant, had an angle of −2.00°. The inside portion better protects the sidewall passivation from angled ion bombardment, and therefore, a more positive angle on the inside is expected and observed.

3. Etch selectivity results

Below are results for, and a discussion on, etch selectivity control using silicon loading, the addition of an oxygen plasma step, wafer electrode power, and wafer temperature. Other parameters such as the effect of passivation and gas flow rates were observed to have minimal effects on etch selectivity and are not described here. The parameters

Table 2
The effects of each parameter investigated on selectivity, silicon etch rate, and profile

Parameter	Silicon loading (%)	Selectivity	Si etch rate (μm/cycle)	PR etch rate (μm/cycle)	Sidewall angle (°) (inside/outside)
Base Etch I	42	75	0.71	0.010	−0.12/−2.00
Base Etch II	57	42	0.73	0.016	−0.05/−1.95
Base Etch III	27	92	0.90	0.010	−0.30/−2.05
Oxygen step	42	30	0.46	0.014	−0.59/−2.01
Higher electrode power	42	55	0.71	0.013	−0.50/−2.16
Lower electrode power	42	103	0.54	0.005	2.34/0.38
Increased temperature	42	48	0.75	0.015	−1.31/−2.93

investigated below are found to coarsely control etch selectivity, enabling gray-scale designs with better precision. Table 2 contains a summary of the effects for each parameter compared to the characteristics of the base etch recipe (Base Etch I). The etch recipes used for the experiments in Table 2 were seen to exhibit similar day-to-day variations in etch characteristics to those commonly observed in other DRIE applications. However, small changes in etch characteristics will exacerbate the problem of precise etch selectivity control in gray-scale technology applications.

3.1. Silicon loading

The effect of silicon loading on etch selectivity was analyzed with a sample having a high silicon loading of 57% exposed silicon (Base Etch II) and a second sample having a low silicon loading with 27% exposed silicon (Base Etch III). In both cases, the exposed silicon was distributed relatively evenly across the wafer, using large features (>50 μm). Local loading effects from various structure sizes in close proximity were not considered. The two samples were then compared to the base etch recipe with a silicon loading of 42%. With a higher loading, etch selectivity decreased to 42 with a silicon etch rate of 0.73 μm/cycle. The lower loading sample had an increased etch selectivity of 92 with a silicon etch rate 0.90 μm/cycle. Additionally, we observed no significant effect on the sidewall profiles. Thus, silicon loading can be used for a coarse control on etch selectivity with minimal effects on the sidewall profiles.

The higher etch selectivity observed for the lowered silicon loading (Base Etch III) is attributed to the proportionality of the silicon etch rate to the available concentration of the Fluorine ions. When the area of the exposed silicon is decreased, the silicon etch rate is increased because the same number of ions are available for etching a smaller area. This increase in only silicon etch rate causes an increase of the etch selectivity. When the silicon loading was increased, the etch selectivity decreased as expected, however the silicon etch rate remained relatively constant. This could be a result of an increase of temperature due to more exothermic reactions taking place. An increase of the etch rate due to increased temperature is balancing the tendency of the higher silicon area to decrease the silicon etch rate. Additionally, the photoresist etch rate of the higher silicon loading was seen to increase by 0.06 μm/cycle which is also attributed to an increased temperature from more exothermic reactions taking place.

One consequence of transferring the photoresist pattern into the silicon that is not present in conventional etching processes is the change of the silicon loading while etching. As the photoresist is removed during etching, more silicon is exposed, increasing the silicon loading. This artifact causes the etch selectivity measurements to be an average value over the entire etch process. The change of silicon loading will depend on the area of the structures being etched. For the test structures in our experiments, the silicon loading changes from 42% in Base Etch I, to 47% by the end of the etch process once the gray levels are cleared. The rest of the wafer is covered by the full thickness of the photoresist and withstands the entire length of the etching. A method of compensating for the change in silicon loading during etching must be investigated to achieve precise, rather than coarse, etch selectivity control.

3.2. Addition of oxygen plasma step

For reducing etch selectivity, an extra step was added in the DRIE process between the etching and passivation steps, using 70 sccm of O_2 without SF_6 or C_4F_8. Etch selectivity was effectively reduced from 75 to 30 while the silicon etch rates changed from 0.71 to 0.46 μm/cycle for a 3 s O_2 step. This step adds another coarse control to decrease the etch selectivity and could be used if changing the silicon loading is not a viable solution. However, this decrease in etch selectivity comes at the price of a slow silicon etching rate. This is possibly due to a native oxide grown on the exposed silicon from oxygen radicals.

Oxygen plasma has long been used as an effective method for the removal of photoresist. In a moderate pressure and high frequency O_2 plasma (ashing), the oxygen atoms attack organic materials forming CO, CO_2, and H_2O that easily desorbs from the surface. Additionally, the reaction between the oxygen and the photoresist is exothermic increasing the surface temperature and the reaction rate. Thus, the primary decrease in the etch selectivity came from a 40% increase of the photoresist etching rate. With a step using 70 sccm of oxygen for 3 s, the photoresist etch rate increased from 0.010 to 0.014 μm/cycle.

3.3. Electrode power

The effect of varying the wafer electrode power was analyzed by choosing powers above and below the power used in the base etch recipe of 10 W. For a lower electrode power (8 W) during the etching cycle only, the etch selectivity increased to 103 and the silicon etching rate decreased to 0.54 μm/cycle. The increased selectivity came from a significant drop in the photoresist etch rate, dropping to 0.005 μm/cycle. For a higher electrode power (12 W) the etch selectivity decreased to 55 with a silicon etch rate of 0.71 μm/cycle, however the photoresist etch rate increased to 0.13 μm/cycle.

These results are due primarily to the change in the amount of material sputtered by ion bombardment. With increased electrode powers, the photoresist etch rate increases because more ions have the necessary energy to physically remove the photoresist, resulting in the lowering of etch selectivity. Even though the silicon etch rate is expected to increase by more sputtering, the increase is small when compared to the overall etch rate, since spontaneous chemical reactions with fluorine is the dominant etching mechanism of silicon. However, by increasing the sputtering, more material is likely to redeposit causing micro masking to occur and rougher surfaces. This can be counteracted by using lower chamber pressures, but at the cost of other characteristics changing, such as sidewall profile.

3.4. Temperature

The Unaxis, Plasma Therm 770 has two primary cooling mechanisms. First, the flow rate of helium across the backside of the wafer is used to control wafer temperature. Second, there is water circulating in the chamber walls, whose temperature is controlled by a water chiller. It is this second mechanism that has been used to influence the temperature of the plasma, indirectly effecting the surface of the sample wafer.

The temperature of the water chiller was changed from 20 to 50 °C, altering the etch selectivity from 75 to 48, respectively. The rate constants for chemical reactions are a function of temperature, as seen with the faster etching rates of silicon (0.75 μm/cycle) and photoresist (0.015 μm/cycle) with the higher temperature. However, due to the faster reaction times, the sidewall passivation is removed quicker and the profile becomes more negative as observed in the results. To counteract this downfall, a longer passivation step may be needed to obtain a more vertical profile.

4. Etch characteristics

4.1. Non-uniformity

The non-uniformity observed in gray-scale technology is significant when compared to planar lithography and transfer techniques. Conventionally, planar processes are used to define all structures. The photoresist defining the structure's planar dimensions is not fully removed when transferring the structure into silicon. Therefore, the top surface of the photoresist where the non-uniformity exists is not transferred in the final silicon structure. In gray-scale technology, however, the photoresist defining the height profile is fully transferred into the silicon. As a result, the non-uniformity in the photoresist thickness can cause structure dimensions to vary across the die and wafer. Additionally, the non-uniformity of the photoresist is scaled by etch selectivity, which can become significant when using a highly selective transfer technique such as DRIE.

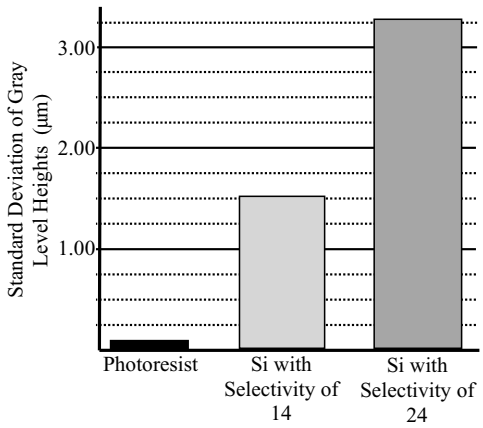

Fig. 5. Bar graph showing the standard deviation measured for a photoresist gray level and a silicon gray level.

Shown in Fig. 5 are the standard deviations of photoresist gray level thickness non-uniformity before etching and the silicon gray level height non-uniformity after etching. Photoresist gray levels, 1.5 μm tall, on five separate samples exhibited an average photoresist thickness standard deviation of 0.13 μm. The non-uniformity of the silicon gray level after DRIE etching was measured for two samples with one having an etch selectivity of 14 (light gray) and the other having an etch selectivity of 24 (dark gray). For both samples the non-uniformity was approximately scaled by the etch selectivity. For instance, the photoresist gray level thickness standard deviation of 0.13 μm, when scaled by an etch selectivity of 24, would yield a standard deviation in silicon of about 3.12 μm, which agrees well with the measured value of 3.25 μm. For a known photoresist non-uniformity, the final silicon non-uniformity can then be estimated by multiplying by the etch selectivity for a chosen recipe. Therefore, using a thicker photoresist layer and a lower etch selectivity can minimize the transfer of the non-uniformity, although photoresist non-uniformity tends to worsen with thicker photoresist layers.

4.2. Surface roughness

A non-contact optical profilometer system was used to analyze the surface characteristics of the gray-scale pattern

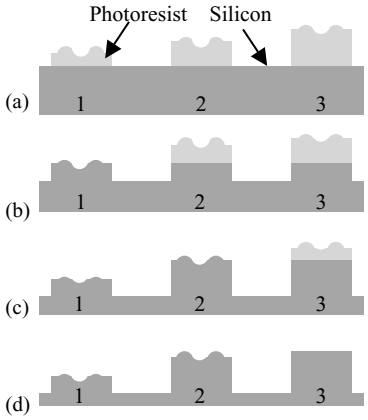

Fig. 6. Steps in the transfer of the photoresist gray levels into the silicon. Structures 1 and 2 are two different gray levels and structure 3 is a conventional (opaque on the optical mask) feature.

transfer using DRIE [20]. Fig. 6 illustrates the method by which the surface roughness of the photoresist is transferred into the silicon surface. In (a) two photoresist gray levels, 1 and 2 and a conventional unexposed photoresist feature, 3, are shown. After some etching, the photoresist gray level A is completely removed and the surface roughness is transferred into the silicon (b). After further etching, the photoresist gray level 2 is completely removed and the surface roughness transferred into the silicon (c). At this point, the silicon gray level 1 continues to be exposed to the isotropic nature of the silicon etching smoothing out some of the surface roughness. After the etching is completed (d), the silicon gray level 1 has been exposed to the isotropic etching longer than gray level 2 allowing the surface of 1 to be smoother than the surface of 2. Meanwhile, structure 3 does not transfer any of the surface roughness into the silicon, since there is still photoresist remaining after the etching completes.

To analyze the surface roughness transfer and the effect of the isotropic nature of the silicon etching, two gray levels were investigated. Before etching, the average roughness of the photoresist gray level surfaces was measured to be below 30 nm. One gray level was etched to a height of 35 μm and had an average surface roughness of 356 nm. The second gray level was etched to a height of 45 μm and had an average surface roughness of 730 nm. The average surface roughness of the unetched silicon was measured to be 15 nm, significantly lower than the roughness measured for the silicon gray levels since the photoresist defining this feature was not completely removed.

Measurements of two samples etched with different etch selectivities to approximately the same depth were also analyzed. From these measurements, the surface roughness depends not only on the original photoresist surface roughness, but also on the etch selectivity as did the non-uniformity. A sample etched with an etch selectivity of 14 exhibited an average gray level roughness of 360 nm (Fig. 7). A sample etched with an etch selectivity of 24 exhibited an average

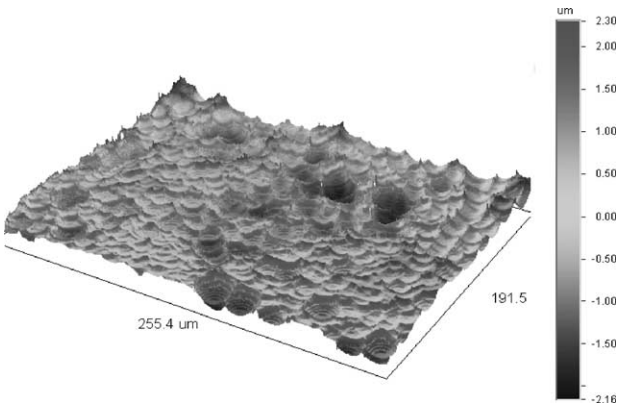

Fig. 7. Surface roughness measurement of a silicon gray level taken by optical profilometry.

gray level roughness of 1.6 μm. This clearly shows a scaling of the surface roughness by the selectivity.

5. Micro-compressor application

Gray-scale technology allows devices to better emulate their macroscopic counterparts, as in the case of the MIT micro Turbine engine device [16–18]. The development of a micro-gas turbine engine requires an efficient compressor design, but current designs have been limited to planar structures using conventional microfabrication techniques as shown in Fig. 8a. A more complex 3D compressor design that improves engine cycle performance is shown in Fig. 8b.

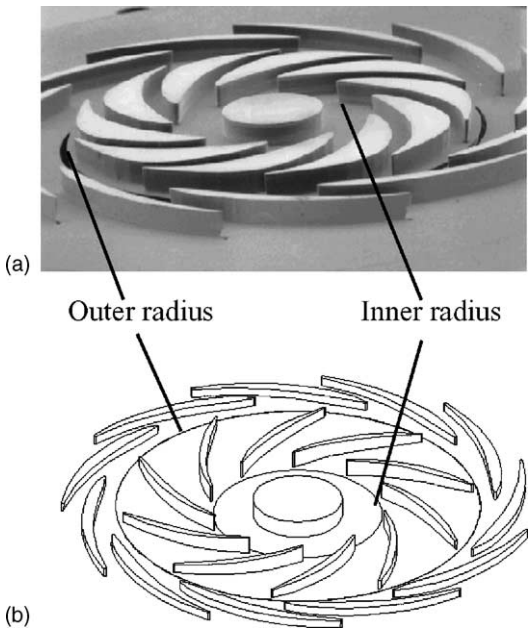

Fig. 8. (a) An SEM image shows a compressor rotor for the MIT micro turbine engine fabricated by planar techniques. (b) A schematic of a rotor shows the preferred taper going from a 200 μm etch depth on the outer radius to a 400 μm etch depth on the inner radius.

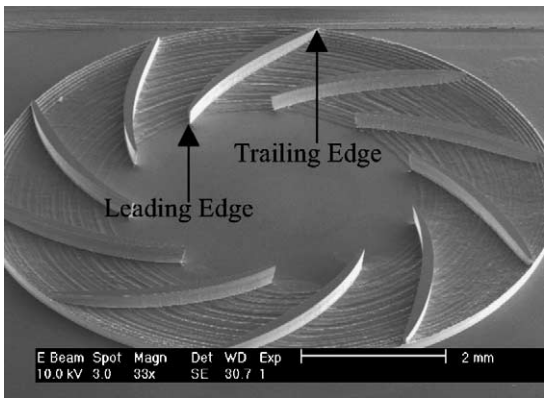

Fig. 9. Variable height micro-compressor in silicon showing the leading edge etched 350 μm and the trailing edge etched 140 μm.

This improved design can be accomplished using gray-scale lithography and DRIE.

The tops of all the blades in the improved design are defined by the original wafer surface and the flow passage bottom wall is etched to a variable depth. To complete the flow passage, another wafer would be bonded to the top of the blades for encapsulation. The flow passage bottom wall slopes from an etch depth of 400 μm at the inner radius to 200 μm at the outer radius. This design allows a mass flow inlet to exit ratio of 2:1 in the vertical dimension.

To obtain the correct height of 200 μm in silicon for the outer-sloped region, the photoresist thickness at the outer-sloped region must be measured so the necessary etch selectivity can be found. For one sample, the photoresist was measured to be below 3 μm so that a selectivity of 67 was needed. When using the Base Etch I from Table 1 a height of 210 μm is achieved. Shown in Fig. 9 is the final silicon micro-compressor using the Base Etch I. The height of the blades is a constant 350 μm above the base of the etched silicon. The height of the sloped region at the outer radius is 210 μm as expected using a selectivity of 75 and a photoresist thickness of below 3 μm at the outer radius. Fig. 10 is a close-up view at the outer radius showing the dimensions of the etched micro-compressor.

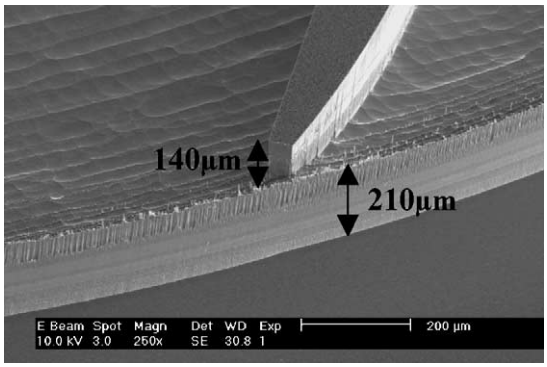

Fig. 10. Close-up of Fig. 9, showing the top of the flow passage wall with a height of 210 μm and a trailing edge blade height of 350 μm.

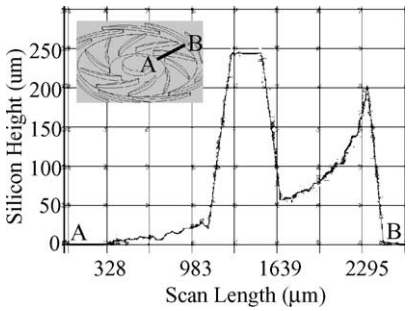

Fig. 11. Contact profilometer scan showing the profile of the compressor with the height of the blade being 245 μm and the height of the slope peaking at 200 μm. The scan goes from A to B in the diagram.

Another demonstration of the micro-compressor used a slightly thicker photoresist layer, where the thickness at the outer-sloped region was measured to be 4 μm. To obtain the designed height of 200 μm in silicon, an etch selectivity close to 50 was desired. An etch selectivity of 52 was obtained by increasing the water chiller temperature to 40 °C and adding 1 s to the etch step. Fig. 11 shows a contact profilometer measurement of the final silicon compressor etched to an average height of 201 μm at the outer-sloped region with a blade height of 245 μm. To obtain the final blade height of 400 μm the sample can continue etching without affecting the sloped profile. This is possible, since the tops of the blades are still protected by the remaining photoresist, while the sloped profile merely continues to be etched deeper into the silicon.

An additional measurement of the final silicon micro-compressor is shown in Fig. 12, using an optical profilometer [20], to compare to the contact profilometer measurement shown in Fig. 11. When using a contact profilometer with a stylus tip, structures with steep sidewalls result in an angled measurement of the sidewall. The measurement of the blade in Fig. 11 exhibits an angled sidewall, but when viewed in an SEM system, the blade appears to have a sidewall angle

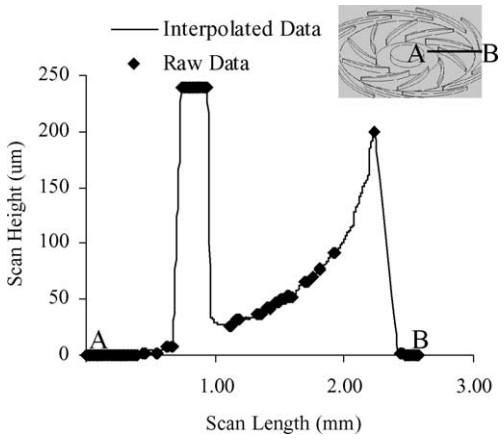

Fig. 12. Optical profilometer scan showing the profile of the micro-compressor showing the raw data and the interpolated data to fill in the missing points. The scan goes from A to B in the diagram.

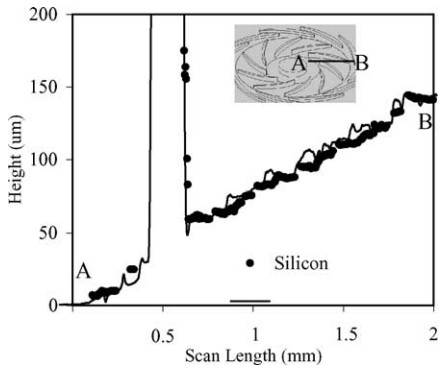

Fig. 13. Two superimposed optical scans show that the profile measured of the etched silicon has a good match with the profile measured in the photoresist (multiplied by an etch selectivity of 75). The scan goes from A to B in the diagram.

close to 90°. This downfall of a contact profilometer causes missing data, since the base of the blade is measured to be almost twice as wide as the top, which we know from SEM micrographs to be false. Use of an optical profilometer can eliminate this problem, however, other effects may cause missing data. In an optical profilometer, steep structures will not reflect light to the CCD camera, causing missing data as seen by the raw data plot in Fig. 12 [20]. For small structures, these problems are insignificant, however, when measuring larger structures such as the micro-compressor they are very apparent. The optical profilometer [20] software has an interpolation function that can be turned on and off which seemingly mimics the data gathered from the contact profilometer. However, the interpolated data must not be confused with true measured data. Both the interpolated and raw data are displayed in Fig. 12. Therefore, using optical profilometry it is difficult to accurately measure the profile of large 3D structures. A combination of profilometer and SEM micrographs is currently necessary.

Fig. 13 shows that an etched silicon profile closely resembles that of the profile defined in the photoresist. Two optical profilometer scans have been superimposed in Fig. 13. The solid line is the measured photoresist profile multiplied by an etch selectivity of 75, while the dots represent the measured silicon profile after etching [20]. There are two possible reasons the etched silicon profile appears smoother than the photoresist profile: first, the small isotropic nature during each etch cycle slowly removes sharp peaks, smoothing the surface as the etch proceeds, and second, the photoresist sample was coated with a 150 Å gold layer to increase reflection, which may slightly alter the measured profile.

6. Conclusions

Proper characterization of photoresist and etched silicon profiles is essential for understanding the capabilities of using gray-scale patterning and DRIE to realize deeply etched 3D silicon structures. Unlike conventional etching using DRIE, precise control over etch selectivity is necessary when transferring gray-scale patterned photoresist into silicon. The results shown in this paper can serve as a guide for tailoring the etch selectivity to the needs of specific gray-scale applications by adjusting process parameters. Of the investigated parameters, silicon loading, the addition of an oxygen step, wafer temperature, and electrode power are used to coarsely adjust the etch selectivity. The ability to control etch selectivity and to minimize the non-uniformity and surface roughness in a DRIE process will allow gray-scale technology to become a powerful microfabrication technology for developing arbitrary 3D silicon structures.

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