INSTITUTE OF PHYSICS PUBLISHING JOURNAL OF MICROMECHANICS AND MICROENGINEERING

J. Micromech. Microeng. **13** (2003) 170–177 PII: S0960-1317(03)52256-2

Investigation of gray-scale technology for large area 3D silicon MEMS structures

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Received 12 August 2002, in final form 11 December 2002
Published 24 December 2002
Online at stacks.iop.org/JMM/13/170

Abstract

Micromachining arbitrary 3D silicon structures for micro-electromechanical systems can be accomplished using gray-scale lithography along with dry anisotropic etching. In this study we have investigated two important design limitations for gray-scale lithography: the minimum usable pixel size and maximum usable pitch size. Together with the resolution of the projection lithography system and the spot size used to write the optical mask, the maximum range of usable gray levels can be determined for developing 3D large area silicon structures. An approximation of the minimum pixel size is shown and experimentally confirmed. Below this minimum, gray levels will be developed away due to an excessive amount of intensity passing through the optical mask. Additionally, oscillations in the intensity are investigated by the use of large pitch sizes on the optical mask. It was found that these oscillations cause holes in the photoresist spaced corresponding to the pitch used on the gray-scale mask and penetrate the thickness of the photoresist for thin gray levels. From the holes in the photoresist, significant surface roughness results when used as a nested mask in reactive ion etching, and the very thin gray levels are lost.

1. Introduction

Micro-electromechanical system (MEMS) designers have traditionally utilized fabrication technologies originating from the mature processes developed for silicon integrated circuit fabrication. However, these processes are primarily dedicated to creating planar structures on the surface or in the bulk of the material such as silicon. Therefore, common MEMS fabrication processes can achieve either vertical sidewalls through dry anisotropic etching [1]; angled sidewalls dependent on the crystallographic orientation of the substrate through wet anisotropic etching [2] or undercut profiles through dry/wet isotropic etching [3]. Conversely, there is an ever-increasing interest in a batch fabrication technique that can realize gradient height profiles in silicon. Such a technique can be utilized to fabricate arbitrary gradient height structures or three-dimensional (3D) structures in silicon that better emulate their macroscopic counterparts, such as small-scale silicon compressors and turbines used in micro-engines [4, 5].

Various 3D fabrication techniques have been demonstrated for the formation of gradient height structures in MEMS devices [6, 7]. Ayón *et al* [8] demonstrated a technique using a buried charged dielectric layer between two silicon substrates in a deep reactive ion etching (DRIE) process to control the path of impinging ions. Another method [9] involves the use of a rotating light source in contact lithography and two masking layers to create a sloped mold for electroplating. Bertsch *et al* [10] have demonstrated a technique by which multiple layers of SU-8 are deposited and patterned individually by combining microstereolithography and thick resist lithography. These techniques, however, either require an unconventional process equipment or are not reproducible as a batch process and therefore, are not widely used for the formation of 3D silicon structures.

A technique using gray-scale lithography has proven to be a useful batch process to create gradient height structures. This method is a one-level lithography process enabling the development of gradient height profiles in a photoresist-masking layer (nested mask) that was used previously for the fabrication of optical elements [11–15]. Whitley *et al* [16] have patented a process by which deep anisotropic etching of silicon can be accomplished by DRIE and/or reactive ion etching (RIE) using gray-scale lithography for the gradient

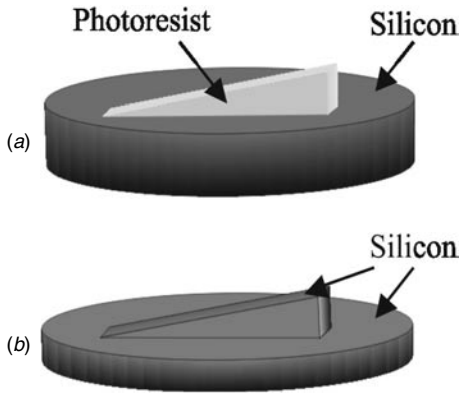

Figure 1. An illustration showing the two primary steps for the fabrication of arbitrary 3D silicon structures using gray-scale lithography to form a nested mask. In (*a*), exposed and developed photoresist from gray-scale lithography for use as a masking layer is shown. In (*b*), the final RIE etched structure in silicon is shown using the masking layer from (*a*).

height-masking layer. However, limited work has been done to characterize the use of gray-scale lithography in fabricating large area MEMS structures with a gradient height profile.

An important aspect of gray-scale lithography is the number of different height levels (gray levels) available to create large area structures in the photoresist and then in the silicon. In this paper we investigate the range of usable gray levels for gray-scale lithography and its use as a nested mask for RIE. Our focus elaborates on the effects of diffraction when using large pitches (center to center spacing between pixels) and additionally, we report on the minimum opaque pixel size that can be used on the gray-scale optical mask.

2. Theory

2.1. Background

The method for the fabrication of gradient height structures in silicon described below consists of two primary steps and is depicted in figure 1. First, the shape of the structure is patterned in a photoresist layer by the use of gray-scale lithography. Second, the photoresist layer is used as a nested mask (multiple height levels) in dry anisotropic etching where the structure is transferred into the silicon substrate to a specified depth corresponding to the height of the desired final structure. Both steps need to be carefully characterized for an overall optimization of this process and its successful implementation as a robust MEMS-based batch fabrication technique.

Gray-scale lithography utilizes locally modulated exposure doses to develop the 3D structure in the photoresist. Differential exposure doses lead to multiple depths of exposed photoresist across the surface. This is due to the ultraviolet light energy being absorbed by the photoactive compound as it travels in the depth of the photoresist. From the differential exposure doses, a gradient height photoresist structure corresponding to the designed silicon structure will remain once developed.

There are two primary techniques to generate an optical mask capable of modulating the intensity passing through to the photoresist surface. One such method uses a high energy beam sensitive glass as an optical mask, in which the glass transmission is changed by an e-beam direct write system [17]. A second method [11] utilizes projection lithography to induce diffraction by using a conventional chrome-on-glass (COG) mask, which can be made by outside mask vendors. The latter method was chosen for our work due to the ease of the mask writing required for the experiment and is described in detail below.

2.2. Diffraction and gray-scale lithography

Diffraction occurs in projection lithography using a COG optical mask patterned with opaque pixels when both the size and the pitch of the pixels are close to or below the resolution of the given lithography system. Here, diffraction is needed to create a modulated intensity pattern or a modulated exposure dose across the surface of the photoresist-covered substrate (aerial image intensity). Figure 2 is an illustration showing diffraction and the resulting aerial image intensity. When diffraction occurs, the light passing through the optical mask breaks up into spatial diffraction orders (+1, −1, +3, −3, etc) and an order (zero) specifying the amplitude or the 'DC' component of the intensity [18]. Once this occurs, the objective lens collects these diffraction orders according to its numerical aperture and will reconstruct the pixels on the photoresist surface if at least the zeroth and one of the first (+1 or −1) diffraction orders are captured as shown in figure 2(*a*). However, when the pixels and spacing between them are small enough (less than the resolution of the lithography system), only the zeroth order is captured by the objective lens and focused onto the photoresist as shown in figure 2(*b*).

The intensity passing through the mask is dependent upon the fill area of each pitch. For instance, if the mask is designed with square pixels and a set pitch between pixels as is shown in figure 3, then the intensity depends on the percentage of the opaque area for each pitch area [12]. In this case the pitch is chosen to be below the resolution of the projection system so that the distance between each pixel remains below resolution. The pixel size can be changed to modulate the intensity passing through the objective lens in the stepper system. Another method to change the intensity is to keep the pixel size constant and change only the pitch, or it is possible to modulate both the pixel size and pitch. For our purposes the first method, keeping a constant pitch and modulating only the pixel size, is chosen for ease in designing the mask. Figure 3 shows a mask with three different pixel sizes and a constant pitch resulting in three different height levels in the positive photoresist structure. Figure 4 is an example photoresist pattern resulting from a similar gray-scale mask [19].

2.3. Design limitations of the gray-scale technology

The primary design issue using gray-scale technology is the number of gray levels, resulting from the different number of intensities, which can be achieved in photoresist. The number of gray levels is then dependent on the resolution and magnification of the projection lithography system, along with the minimum pixel size and increment between subsequent

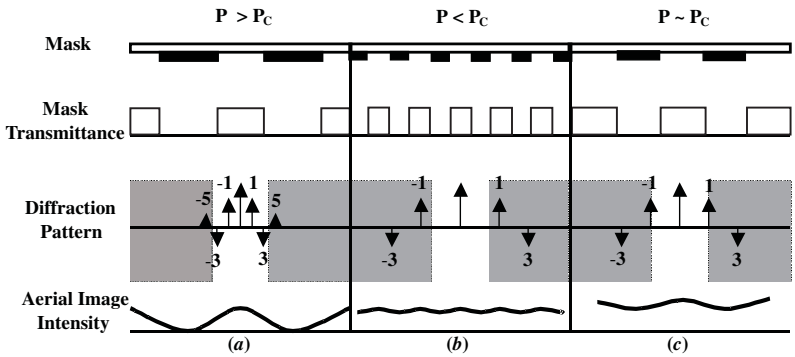

Figure 2. Illustration showing behavior of diffracted light assuming the critical pitch P_C is the smallest pitch where the numerical aperture accepts one of the first diffraction orders. Diffraction orders in the shaded region denote the orders not accepted by the numerical aperture of the objective lens in the lithography system.

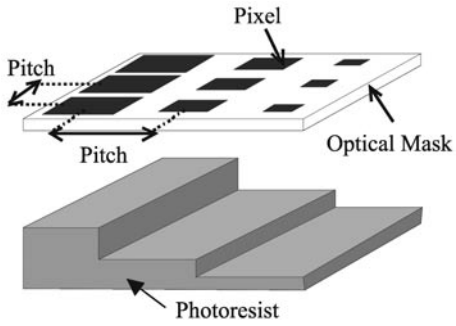

Figure 3. Example of a three-level gray-scale mask pattern and the resulting photoresist structure.

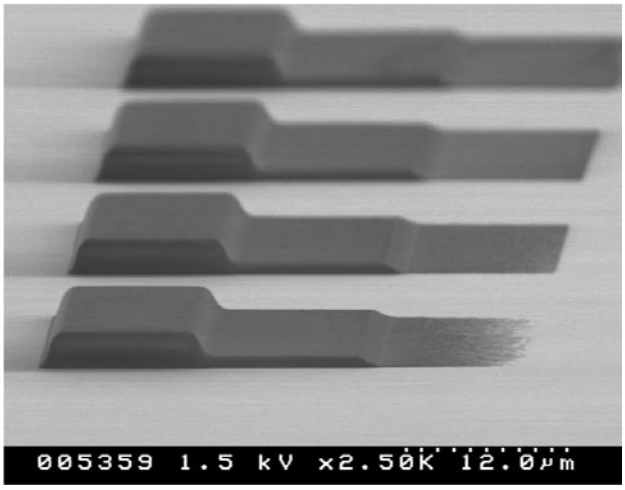

Figure 4. Three gray levels patterned in AZ 4620 photoresist resulting from a similar mask pattern in figure 3.

pixel sizes used to create the gray-scale mask. The number of gray levels, in turn, determines the roughness or exact definition of the profile in the photoresist.

There is a resolution limit on the minimum pixel size for a given projection lithography system, which sets the upper limit for the area of all features and spacing on the optical mask. Therefore, due to the diagonal spacing between two pixels being the largest spacing, an approximation of the minimum pixel size can be shown by the equation

$$w_{\min} = P - \sqrt{\frac{P_C^2}{2}} \tag{1}$$

where $w_{\min}$ is the minimum pixel width, P is the pitch chosen for the mask and P_C is the resolution of the projection system being used. The diagonal spacing becomes above the resolution when pixel widths below $w_{\min}$ are used. An excessive amount of intensity will then pass through the optical mask and cause the photoresist to fully develop. The minimum and maximum pixel size (up to the pitch size used), and the minimum e-beam write size pertaining to a given pitch, will ultimately set the number of gray levels that one will achieve.

The photoresist structure size, such as length, is correlated to the number of gray levels available, for a desired smoothness, and the size of the pitch used to create the gray-scale mask. The maximum number of gray levels is fixed for a particular lithography system, via a specific method of creating various fills within a set pitch and given the minimum e-beam write size for the gray-scale optical mask. Alternatively, the pitch can be changed to vary the size of the structure, such as increasing the length by increasing the size of the pitch. However, oscillations in the aerial image intensity, corresponding to the partial reconstruction of the mask pattern, will occur if a pitch is equal to or just above the resolution of the projection lithography system (shown in figure 2(*c*)). When the pitch is large enough (above resolution), the oscillations become the actual pattern reconstructed in the photoresist. This is of interest, because larger pitch sizes can be used to develop structures with a larger area in the photoresist with a given number of gray levels. Experiments have been carried out to investigate the use of larger pitches and their effects on oscillations during the lithography and subsequently on the etching of the final structure.

A calibration mask with multiple gray-scale patterns of different pitches and with all available pixels (available for mask production) can be used to find both design limits (the minimum pixel size and maximum usable pitch size) for a specific type of photoresist. In addition to these limits, it is necessary to learn the final photoresist height of the individual gray levels, which can be done using the same calibration mask. The heights of the gray levels depend on many factors, primarily the initial photoresist thickness, the aerial image intensity for each gray level, the absorption coefficient

(including the Dill parameters describing properties of the photoresist) which ultimately gives the concentration of both the photoactive compound remaining and exposure product produced, the time of development and the contrast of the photoresist. The calibration mask can be used to characterize all different photoresist types and their thickness.

Simulation programs and analytical models used for projection photolithography can aid in the design; however, due to different lab environments, the parameters will still need to be adjusted by the use of a calibration mask. Therefore the primary use of such programs or models is for the optimization of the process and required experimental steps. Conventional lithography has the same procedure of calibrating the process parameters for new photoresist films.

Once the gradient height photoresist structure is formed, it can be used as a nested mask in dry anisotropic etching to transfer the pattern into the underlying silicon substrate. For relatively shallow depths, RIE etching is used. The important etch parameter governing the desired silicon structure is the selectivity of the etch process or the etch rate of the silicon versus the etch rate of the photoresist. For this reason it is important to be able to control the selectivity of the RIE etch in this process.

3. Experiment

The gray-scale mask layout was designed using a conventional layout editor (AutoCAD and ICED). The minimum pixel size is 0.4 μm on the mask with a 0.1 μm consecutive increment size between two pixel levels. The mask was a chrome-on-quartz mask purchased from a commercial vendor. A wafer stepper (GCA Ultratech) was used for the exposure having a resolution limit of about 0.7 μm, a magnification of 5 and an exposure wavelength of 365 nm. An RIE system from Trion Technologies was used to anisotropically etch the patterns into silicon.

Given the estimated resolution of the stepper, a minimum pitch of 0.7 μm on the wafer or 3.5 μm on the mask was chosen. Various test patterns with pitches of 3.5 μm, 4.0 μm and 5.0 μm were drawn on the mask. These pitches were chosen to be at and just above the resolution of the wafer stepper allowing the investigation of the effect the intensity oscillations have on both lithography and RIE etching. Numerous sizes of wedge-like test structures are included on the mask, having one, two, five or ten rows of the same pixel size for each gray level.

For this experiment, two types of positive thick photoresist, AZ 4620 and AZ 9245, were used. Both resists can be spun up to 20 μm in thickness. AZ 4620 photoresist is a low contrast resist in comparison with AZ 9245, which has a higher resolution. Analysis of the photoresist profiles and RIE etching comes from both SEM visual measurements and profilometer readings.

4. Results and discussion

4.1. Gray-scale lithography

Figure 5 shows the layout of the mask developed in a 5 μm thick AZ 4620 photoresist and the test structures that were investigated. The largest structure (on the left-hand side of the optical micrograph) was designed to be 500 μm long and 100 μm wide in the photoresist. This structure consisted of a 5.0 μm pitch with ten rows per pixel size and 45 gray levels on the mask. The smallest structure was designed to be 25 μm long and 35 μm wide on the mask, consisting of a 3.5 μm pitch with one row per pixel size and 30 gray levels. The different shadings in the structures correspond to different heights in the photoresist layer. The calculated number of height levels expected for each pitch size in the photoresist was 24, accounting for the minimum allowable pixel width calculated from equation (1), using 3.5 μm for P_C.

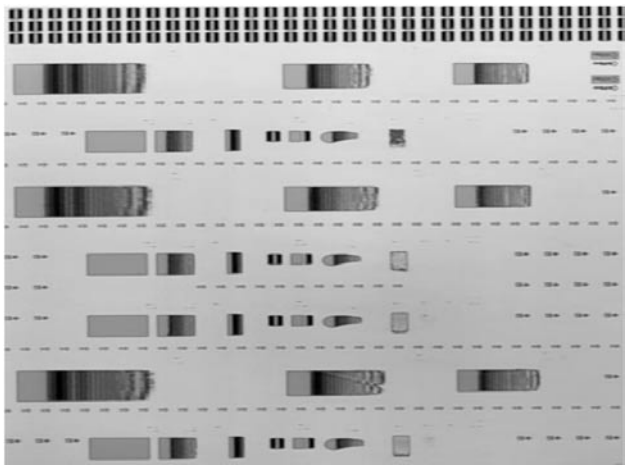

Figure 5. An optical micrograph showing a top down view of the gray-scale mask layout developed in AZ 4620 photoresist.

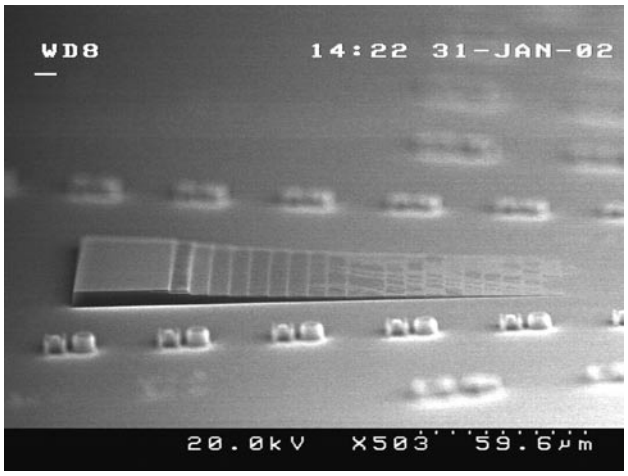

Figure 6. An SEM image of AZ 4620 developed photoresist consisting of 22 height levels using a 3.5 μm pitch on the mask and ten rows per pixel size.

Figure 6 shows a close-up view of a gray-scale profile in AZ 4620 photoresist using a 3.5 μm pitch, with ten rows per pixel size. The exposure dose was 350 mJ cm^{-2} and an absolute focus setting of 0 was used. From this, 22 gray levels were obtained. In contrast, a maximum of 19 gray levels was achieved in AZ 9245 photoresist with the given mask, an exposure dose of 594 mJ cm^{-2} and a focus of zero. The difference in the number of gray levels between the two experiments is attributed to the difference in the absorption and contrast characteristics of each photoresist. AZ 4620 has lower

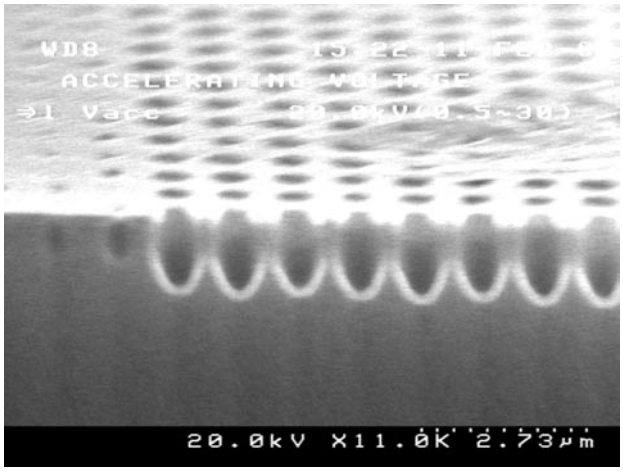

Figure 7. SEM image showing holes in an upper gray level developed in AZ 9245 photoresist due to the partial recreation of the features.

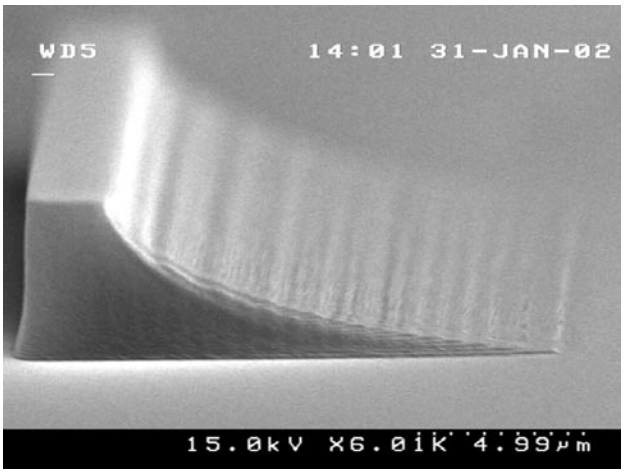

Figure 8. SEM image showing developed AZ 4620 photoresist using a 3.5 μm pitch and one row per pixel size.

contrast, allowing higher intensity levels to still be resolved. As expected, not all 30 of the gray levels were developed, due to the minimum pixel size requirement. We attribute the loss of some levels from the expected number, 24, to the need for good control on the development time and developer concentration as well as the need to have a uniform intensity source (incident on the optical mask in the wafer stepper) across the entire die and wafer. In addition, the number of gray levels is dependent on the exposure dose. Therefore, an optimum exposure dose was chosen due to the maximum number of gray levels achieved.

The effects of the intensity oscillations from the use of large pitches can be seen in figure 7. This results in holes that can easily be observed in the photoresist layers for all gray levels. The spacing between the centers of each hole is the same as the pitch used on the mask and corresponds to the diagonal spacing between the pixels. The intensity forming the holes does not appear to penetrate the entire thickness of the photoresist for the thicker gray levels. However, for the thinnest gray levels, it appears that the holes do penetrate to the surface of the silicon. This ultimately hinders the ability to achieve the lower gray levels when combined with the higher intensity already existing from the large diagonal spacing from the use of very small pixel sizes.

Figure 8 shows a close-up of the smallest structure on the mask, using a 3.5 μm pitch, with only one row per pixel size. In this image a non-linear height profile is exhibited and is the result of the aerial intensity transfer equation, described in [12], the absorption of energy by the photoactive compound in the depth of the photoresist and the development rate equations, all being non-linear processes. Correction for the non-linearity can be made in the design of the gray-scale optical mask [15]. There are no holes apparent in these structures that consist of only one row per pixel size. Although it is difficult to count the number of levels achieved in this structure, it seems that the lowest or thinnest gray level achieved is the same as for other structures, making this structure not totally immune to the intensity oscillation effect.

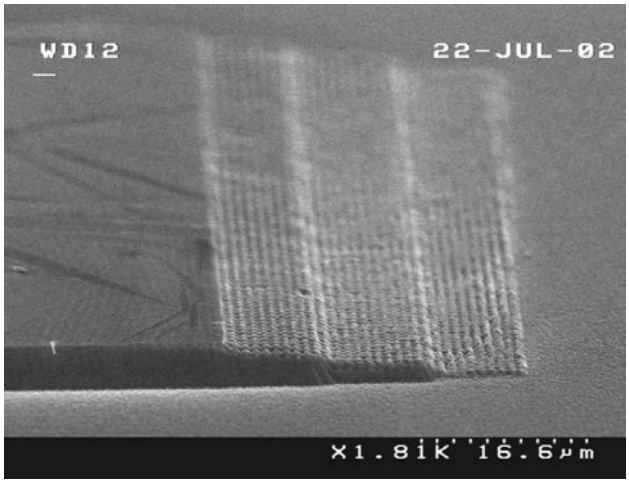

Figure 9. SEM image of an etched silicon structure 9 μm tall resulting from a gray-scale nested mask and RIE etching using a pitch of 5.0 μm and ten rows per pixel size.

4.2. RIE etching

For the investigation on the effect the holes in the photoresist have in the transfer of the pattern into silicon, RIE etching was used with a controlled selectivity. The selectivity in this process along with the silicon etch rate ultimately determines the depth of the structure and the heights of the individual gray levels. For this study, the oxygen flow rate was used to help control the selectivity of the etch process. Oxygen is used for the passivation of the sidewalls, allowing an anisotropic etch process using SF_6 as the silicon etchant. Additionally, oxygen plasma is an efficient etchant of organic materials that can reduce the selectivity by increasing the photoresist etch rate.

The holes in the photoresist-masking layer result in a large surface roughness on the individual gray levels when etched. Figure 9 shows an etched silicon structure corresponding to the photoresist structure shown in figure 6. The etching was stopped before the photoresist was fully removed, allowing only four distinct gray levels to be developed in silicon. A close-up of the surface of the larger gray levels is shown in figure 10. It can be seen that the surface roughness is in

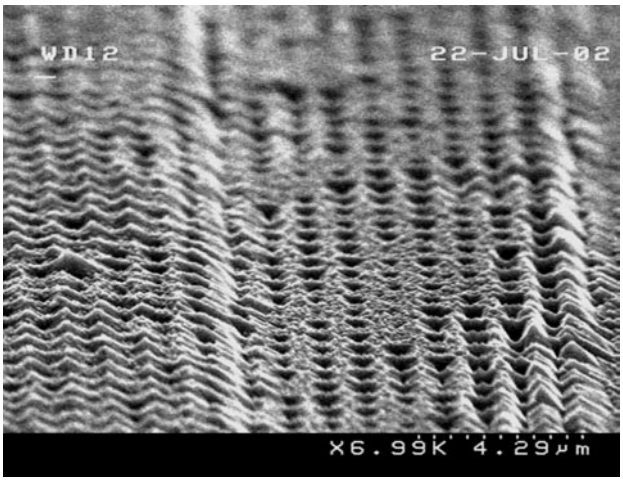

Figure 10. SEM image of the thicker gray levels etched in the silicon corresponding to the structure shown in figure 9. This SEM shows the surface roughness, which comes from the holes in the photoresist layer due to the intensity oscillations.

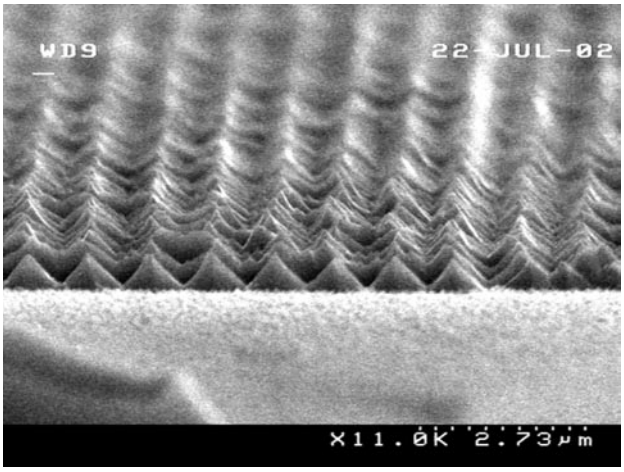

Figure 11. SEM image of the lowest gray level corresponding to the silicon structure in figure 8. The spaces between the spikes seem to reach the surface of the silicon that was not masked by photoresist.

the form of spikes spaced periodically corresponding to the pitch used and the holes in the photoresist. Figure 11 is an SEM image of the lowest gray level, which shows the spikes more clearly. It appears that in this level, the holes between the spikes reach the surface of the silicon not covered by photoresist. The etch recipe in this experiment used 33% oxygen and 67% SF_6 flows, a pressure of 200 mTorr, an electrode power of 100 W, with a selectivity close to 2.75. The final etched structure was 9 μm tall giving an etch rate of about 1.4 μm min^{-1}.

Another etch recipe with a larger selectivity of about 5.3 and a lower pressure of 150 mTorr was used. With this, the etching rate of the silicon and the photoresist increased and more levels were etched in the same amount of time. Figure 12 shows the SEM image of the same structure as before, resulting from this different etch recipe. Figure 13 is a close-up of the upper levels in which the surface roughness was less and the periodicity corresponding to the pitch was lost. This was in part due to a lower chamber pressure allowing for etch

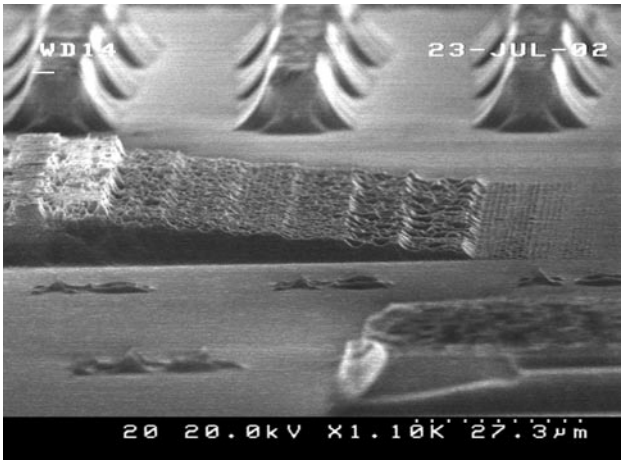

Figure 12. SEM image of a silicon etched structure about 11 μm tall resulting from a higher selectivity and a lower chamber pressure etch. A total of ten gray levels were achieved using this etch.

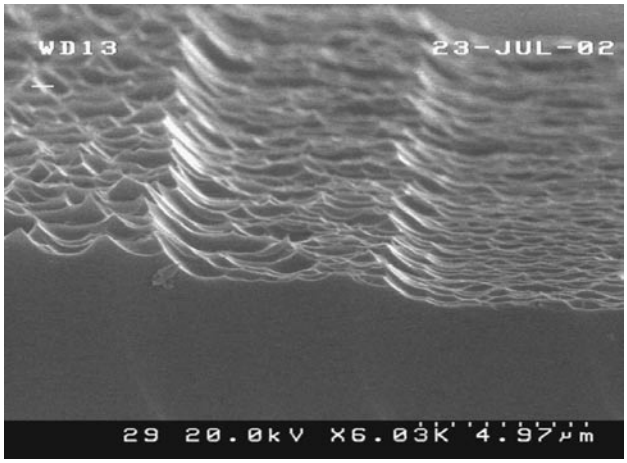

Figure 13. SEM image showing a close-up view of the upper levels that are shown in figure 12. From the etch process used, the roughness has been decreased and there are no periodic spikes.

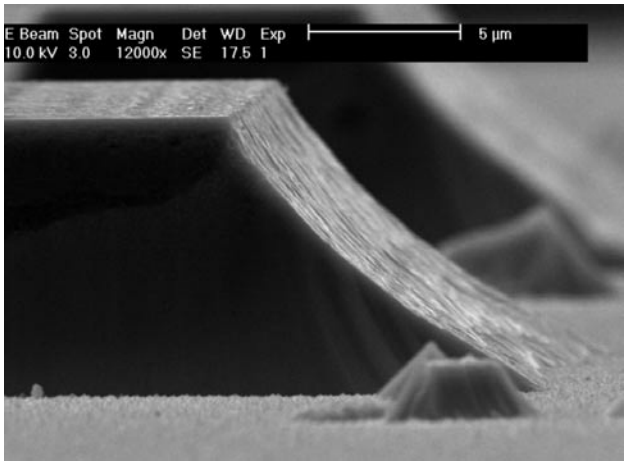

Figure 14. SEM image of an etched silicon structure resulting from a gray-scale nested mask and RIE etching using a pitch of 3.5 μm and one row per pixel size.

volatiles to be removed more effectively. Also with a lower chamber pressure used, ion bombardment is reduced and the

etch process exhibits a more isotropic behavior allowing the spikes to be etched away. However, from this etch the lower gray levels were lost, leaving only small scattered spikes shown on the very right side of the structure in figure 12.

Figure 14 shows an RIE etched silicon structure corresponding to that in figure 6. The selectivity of this etch was 1.3 and a depth of 8.4 μm was achieved. This profile exhibits a fairly smooth surface when compared to the larger features etched as in figure 9. As before, the etching was stopped before the photoresist was etched completely, not allowing all levels to be etched into the silicon.

5. Conclusions

The advantage of gray-scale technology is the development of 3D structures formed using conventional batch fabrication methods by simply changing the optical mask pattern to create a gradient transmission during lithography. Multiple height levels (gray levels) are thereby developed in a photoresist-masking layer for silicon dry anisotropic etching. In this paper, the range of usable gray levels was investigated and reported to better understand the limits for the application of gray-scale lithography in designing 3D MEMS silicon structures.

An approximation to the lowest gray-level resolvable, due to the criterion of the minimum pixel size, was found and experiments show that this holds quite well. The result of this is the loss of gray levels in the photoresist. With the given mask design, 24 gray levels (out of more than 30 gray levels designed on the gray-scale mask) were approximated to be resolved. In the experiments, the gray levels achieved were 22 using the AZ 4620 photoresist and 19 using the higher resolution AZ 9245 photoresist, showing that the approximation is close. Once the minimum pixel is found, it can be accounted for in the design of the gray-scale mask.

Along with the lowest gray-level resolvable, the resolution of the projection lithography system and the increment used between different pixel sizes determines the number of gray levels possible for that system. This gives a limit to the total area that the structure can span for a given pitch. Therefore, the largest pitch size would be ideal giving the largest area structure using only a single row of pixels per gray level. We investigated and described in detail the effects of using pitch sizes above the resolution of the projection lithography system. This causes large oscillations in the aerial intensity resulting in the formation of holes in the photoresist-masking layer. In addition to the large surface roughness in the etched silicon, the thinnest gray levels were lost due to total penetration of the holes in the photoresist to the silicon surface below. Hence, pitches below the resolution of the projection lithography system, where the intensity oscillation is minimized, should be used for the smoothest profiles. However, it should be noted that the surface roughness is less significant when the pitch is close, but still above the resolution of the lithography system and therefore could be used depending on specified roughness tolerances. For large area silicon MEMS structures fabricated by gray-scale technology, the maximum usable pitch size can be found and the number of pixels per gray level can be maximized for further designs.

The two important design parameters, the minimum usable pixel size and maximum usable pitch size, reported in this paper are key process elements for an optimized and robust gray-scale lithography process. This technique combined with dry anisotropic etching is a promising micromachining technology for batch fabrication of large area 3D silicon structures in MEMS devices and systems.

Acknowledgments

The Army Research Laboratory (ARL) Collaborative Technology Alliance (CTA) Power and Energy program supports this project. The authors would like to thank Rohit Grover and Toby Olver for their help in using the wafer stepper at the Laboratory for Physical Sciences (LPS) of the National Security Agency (NSA) in College Park, MD. The test structures were fabricated in the cleanroom facilities at both ARL in Adelphi, MD and University of Maryland in College Park. Christopher M Waits is a fellow under the Graduate Assistance in the Areas of National Need (GAANN) program funded by the US Department of Education.

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