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Residual stress and fracture in thick tetraethylorthosilicate (TEOS) and silane-based PECVD oxide films

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Abstract

This paper reports residual stress measurements and fracture analysis in thick tetraethylorthosilicate (TEOS) and silane-based plasma enhanced chemical vapor deposition (PECVD) oxide films. The measured residual stress depended strongly on thermal process parameters; dissolved hydrogen gases played an important role in governing intrinsic stress. The tendency to form cracks was found to be a strong function of film thickness and annealing temperature. Critical cracking temperature was predicted using mixed mode fracture mechanics, and the predictions provide a reasonable match to experimental observations. Finally, engineering solutions were demonstrated to overcome the problems caused by wafer bow and film cracks. The results of this study should be able to provide important insights for the design of fabrication processes for MEMS devices requiring high temperature processing of films.

Keywords: PECVD oxide films; Residual stress; Fracture

1. Introduction

Plasma enhanced chemical vapor deposition (PECVD) is an important thin film process for the fabrication of microelectronic devices and microelectromechanical systems (MEMS). Because PECVD is facilitated by plasma rather than by high temperature, it is widely used in applications with low thermal budgets or requiring fast deposition rates. Recent MEMS devices such as micromotors are pushing electrical and mechanical power requirements to higher levels [1,2]. Higher power applications require thicker deposited layers, for example as electrical insulation or mechanical flexures. However, the ability to deposit films with thicknesses significantly greater than a few microns is limited by residual stress, which can result in substrate distortion or even cracking of the film or substrate. These stress problems increase with film thickness.

The present work was motivated by the process integration of a micromotor driven compressor device [3,4]. Fig. 1 shows a die-level picture of a stator for the micromotor compressor. The micromotor must have high power density and must operate at high efficiency. This places several requirements on the electrical stator. First, it must operate at high voltages (~300 V) without electrical breakdown. Second, the electrodes and interconnects must be well insulated from the substrate to minimize capacitive loading. Finally, the process must lead to a planar, unbowed surface to permit wafer bonding and to ensure a 3 μm air gap between the rotor and stator.

To meet these requirements, the stator electrical elements must be fabricated on top of a thick, high quality oxide film. To achieve this, two goals in film fabrication had to be met. First, sufficient thickness (typically, greater than 10 μm) was required in order to reduce capacitive loading. Second, the breakdown strength of the insulating film had to be able to withstand the high applied electrical loads. In order to achieve the first goal, PECVD oxides were chosen for the high deposition rate. After deposition, oxide films were subjected to a high temperature (typically 1100°C) densification to achieve better electric breakdown strength. Depositing oxide films with the required thickness was not difficult, however, after densification, the wafer exhibited excessive distortion and cracks were found in the film if the film thickness exceeded 15 μm [5]. The deleterious effects of residual stress that tend to increase with thickness are a prime limitation to the deposition of very thick films. Since wafer distortion and film cracking both seriously impact MEMS process integrity and device reliability, it is important to elucidate the factors contributing to residual stresses in oxide films and to optimize the deposition process so as to reduce wafer bow and to avoid film cracking.

The present work focused on the residual stress characterization and fracture analysis in thick tetraethylorthosilicate

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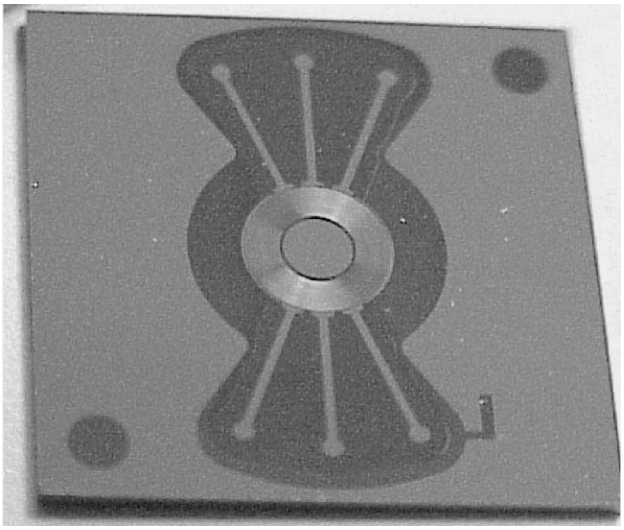


Fig. 1. Optical photograph of a motor compressor stator after thin film processing.

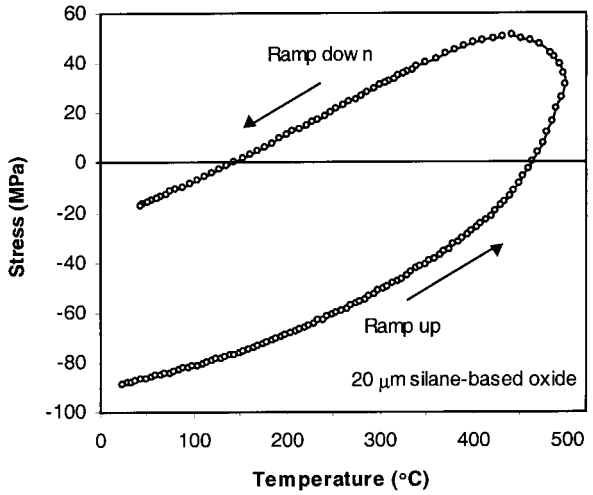


Fig. 2. Residual stress and wafer bow variation of 20 μm thick silane-based PECVD oxide film as a function of temperature during a 500°C thermal cycle.

(TEOS) and silane-based PECVD oxide films. Conformality of TEOS-based oxide in high aspect ratio features has been found to be better than that achieved by other means of growing/depositing oxide [6]. The aim of this work is to provide a fundamental understanding on the residual stress behavior and fracture mechanics of thick oxide films.

2. Deposition and characterization

Both silane and TEOS-based PECVD oxide films were deposited using a five-station continuous plasma processing system (Concept One, Novellus Inc.) [7]. The deposition was conducted on four inch, 500 μm thick wafers all from the same batch of ⟨1 0 0⟩ orientation boron doped wafers. Film thickness varied from a few microns to a few ten microns. The nominal gas flow rates of silane-based oxide are 300 sccm of SiH_4, 9500 sccm of N_2O and 1500 sccm of N_2. The deposition was performed at 400°C with deposition rates of the order of 1 μm/min. TEOS-based oxide was deposited at a relatively low temperature, 350°C. The nominal gas flow rates are 2.3 ml/min of TEOS and 9500 sccm of O_2. The deposition rate of TEOS-based oxide is nominally 0.25 μm/min. In all the cases the wafer-level thickness, deposited on a 4 in. wafer, has non-uniformity less than 1%. However, there is a 3% reduction in film thickness across the wafer after densification.

Thermal cycling tests were conducted in order to assess the role of temperature dependent effects in determining the state of residual stress in the films. Thermal cycling of a variety of films with a heating rate of 1–5°C/min was conducted. In situ wafer curvature was measured between room temperature and 500°C using a KLA-Tencor™ FLX-2320 system. The corresponding residual stress was calculated, as a function of temperature, using the Stoney equation [8]:

$$\sigma_f = \frac{E_s h_s^3}{6(1-\nu_s)Rh_f^2(1+h_s/h_f)} \quad (1)$$

where $1/R$ is the curvature, h_s and h_f are thickness of substrate and film, respectively. E_s and ν_s are Young's modulus and Poisson's ratio of the substrate. Eq. (1) was derived from bimaterial laminated plate theory and has been installed in the testing system for data conversion. Fig. 2 shows the residual stress and the corresponding wafer bow for a 20 μm thick silane-based PECVD oxide film as a function of temperature during a thermal cycle between room temperature and 500°C. The dependence of residual stress on temperature is clearly non-linear with significant hysteresis.

PECVD process utilized a plasma to overcome the chemical inertness at low temperature. As a result, many radicals and intermediate species still existed after reaction. Previous investigation indicated that the hydrogen atoms or silicon–hydrogen bonds make important contribution on the intrinsic stress of PECVD films [9]. For this reason, a high temperature densification process was incorporated as a standard approach to minimizing this problem. Hydrogen concentrations of oxide films at various stages were measured. Typical hydrogen contents of both as-deposited TEOS and silane-based PECVD oxide films are in the range of 3–5 at.%, as measured with Rutherford backscattering spectroscopy (RBS). Subsequent densification was accomplished by subjecting the films to a higher temperature for 1 h while a steady N_2 flow was maintained in the furnace. Table 1

Table 1
Hydrogen concentration of PECVD-TEOS-based oxide films

T (°C)	350	700	800	900	1000	1100
H_2 (%)	4.00	0.67	0.13	0.20	0.17	0.17

tabulates the hydrogen content in 1 μm TEOS-based oxide films in six different conditions: as deposited, and after 1 h densification at 700–1100°C. The hydrogen content in TEOS-based oxide films falls below 0.2% after densification at temperatures higher than 800°C.

3. Results and discussion

3.1. Residual stresses and deformation

In general, for thin film processes, residual stress is the sum of thermal and intrinsic stresses. Thermal stress develops in thin films when high temperature deposition or high temperature annealing are involved. Due to the difference in thermal-mechanical properties between the film and substrate, thermal stress is usually unavoidable. Intrinsic stress is generated during film growth and is strongly dependent on process conditions. In order to understand the behavior of intrinsic stress, the thermal stress component must be subtracted from the measured residual stress. For simplicity, thermal stress can be estimated based on the assumption of constant material properties. If the film is deposited at a temperature T_1 when heated or cooled to a different temperature T_2, the thermal stress in the film becomes

$$\sigma = \frac{(\alpha_f - \alpha_s)(T_1 - T_2)E_f}{1 - \nu_f} \quad (2)$$

where E_f and ν_f are Young's modulus and Poisson's ratio of the film, and α_f and α_s the thermal expansion coefficients of film and substrate, respectively.

By using the literature values of 70 GPa for $E_f/(1-\nu_f)$, $0.5 \times 10^{-6}\,K^{-1}$ for α_f and $3 \times 10^{-6}\,K^{-1}$ for α_s, thermal stress in 20 μm thick silane-based PECVD oxide film was calculated. Fig. 3 shows the decomposition of thermal stress and intrinsic stress for the data given in Fig. 2. Apparently, the variation of stress with temperature is due to two superimposed effects: a linear thermal stress component, and a non-linear, irreversible intrinsic stress component.

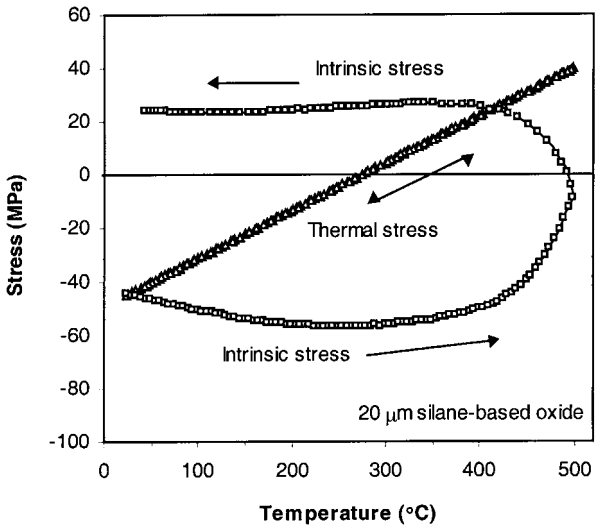
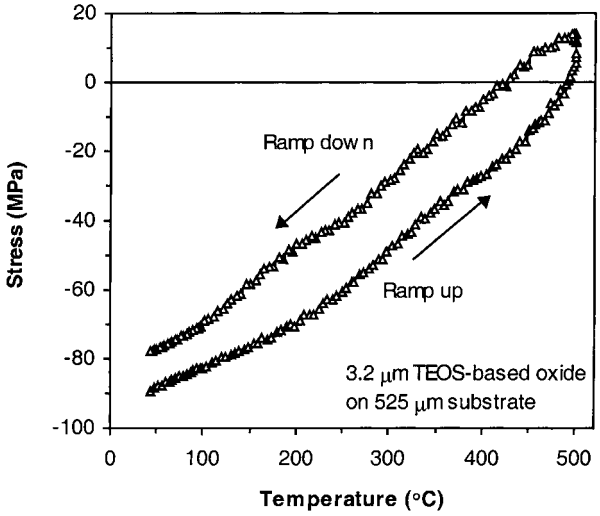
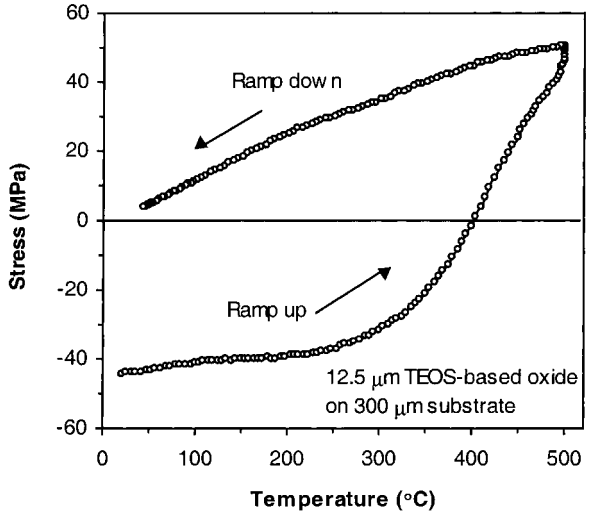


Fig. 3. Decomposition of thermal stress and intrinsic stress in 20 μm thick silane-based oxide film as a function of temperature during a 500°C thermal cycle.



(a)



(b)

Fig. 4. Residual stress variation of TEOS-based oxide film as a function of temperature during a 500°C thermal cycle: (a) 3.2 μm thick TEOS-based oxide film on 525 μm silicon substrate; (b) 12.5 μm thick TEOS-based film on 300 μm silicon substrate.

Similar behavior exists in TEOS-based PECVD oxide films. Residual stress variation with temperature in thick TEOS-based oxide films is given in Fig. 4. Fig. 4(a) shows the residual stress in a 3.2 μm thick TEOS-based oxide film with a 525 μm standard silicon substrate while Fig. 4(b) gives the residual stress variation in a 12.5 μm thick TEOS-based oxide film with a 300 μm silicon substrate. Residual stress as a function of temperature in TEOS-based oxide films exhibited a similar non-linearity with hysteresis behavior during the thermal cycle between room temperature and 500°C, and the hysteresis loop indicates that the intrinsic

stress of TEOS-based oxide was permanently changed after thermal cycling.

There are many mechanisms that may be responsible for the generation of intrinsic stress. Typical examples include incorporation of atoms (e.g. residual gases), chemical reactions, recrystallization, dislocation rearrangements, lattice mismatch, excess vacancy annihilation, grain boundary relaxation, and phase transformations [10]. In the present case, given that the RBS analysis of oxide films shows two orders of magnitude difference in hydrogen concentration before and after annealing, it is likely that the initial compressive intrinsic stress might be caused by dissolved gases. Since oxide films were deposited at low temperature, lack of surface diffusivities of molecules may lead to some extent to considerable porosity [11]. As temperature increased, residual gases were driven out due to increase in chemical potential. In addition, the surface diffusivities of solid structure were also enhanced. Shrinkage then occurred in order to reduce the surface energy, and tensile stress was generated. The tendency towards shrinkage retains as temperature decreases.

Additionally, thermal cycling experiments were conducted on silicon nitride films. PECVD nitride was deposited at 400°C while LPCVD nitride deposition was conducted at 840°C. Residual stress and wafer bow behavior of the nitride films under thermal cycling are shown in Fig. 5. Compared to 1 μm thick PECVD nitride thermal cycling curves given in Fig. 5(a), 0.25 μm LPCVD nitride (Fig. 5(b)) exhibited virtually no hysteresis. This further confirms the above arguments about the sources of intrinsic stress. PECVD films normally have very high concentrations of residual gases, and therefore, the intrinsic stress is believed to be strongly correlated with the impurities existed inside the films and the ion bombardment produced by the deposition processes.

Furthermore, the densification step plays an important role in determining stress and wafer bow in oxide films. The room temperature residual stress with annealing temperature in 3.2–11.5 μm TEOS-based oxide films is given in Fig. 6. Obviously, the room temperature residual stress became more compressive as annealing temperature increased. Fig. 7 shows room temperature wafer bow versus film thickness, before and after 1100°C densification. It is seen that the compressive residual stress observed at room temperature increases significantly after the annealing process. Wafer bow in densified TEOS-based oxide films is much larger than that of the as-deposited films. This is most likely due to thermal stress, as oxide at such temperature levels (higher than 900°C) becomes viscoelastic and stress-free. Residual stress can be gradually relieved by material flow, as the temperature increases. As a result, the stress in oxide films becomes more compressive when cooled from high densification temperature to the room temperature.

3.2. Fracture

Both silane and TEOS-based oxide films were observed to crack after being exposed to the annealing cycle. The

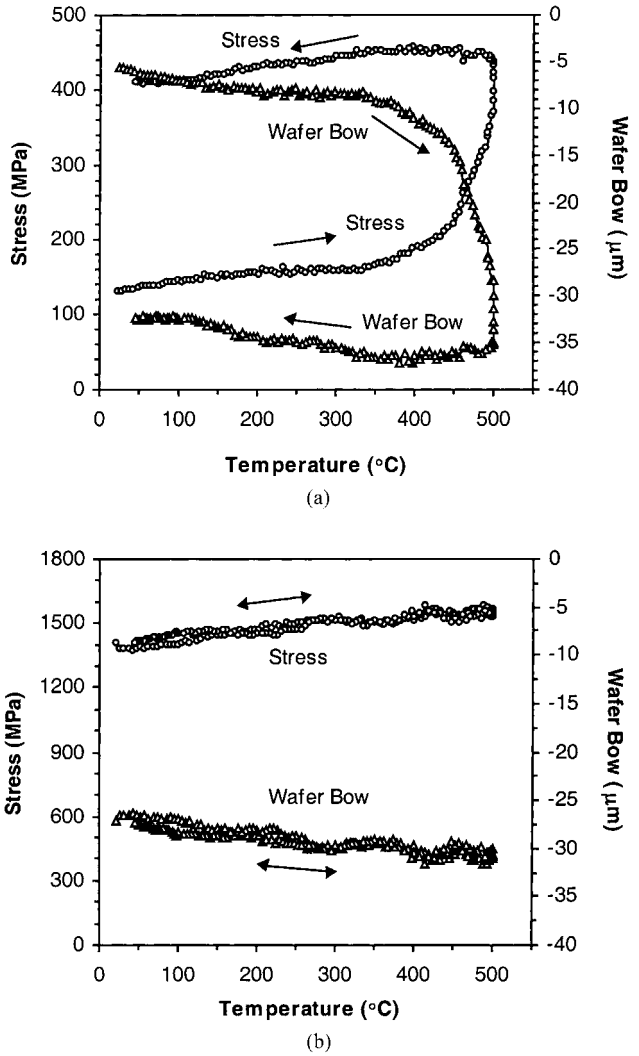


Fig. 5. Residual stress and wafer bow variation with temperature for silicon nitride films: (a) 1 μm thick PECVD nitride films; (b) 0.25 μm thick LPCVD nitride films.

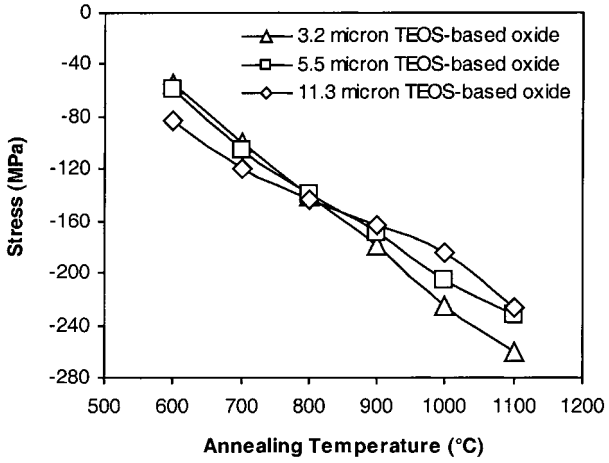


Fig. 6. Variation of room temperature measured residual stress with annealing temperature in thick TEOS-based oxide films.

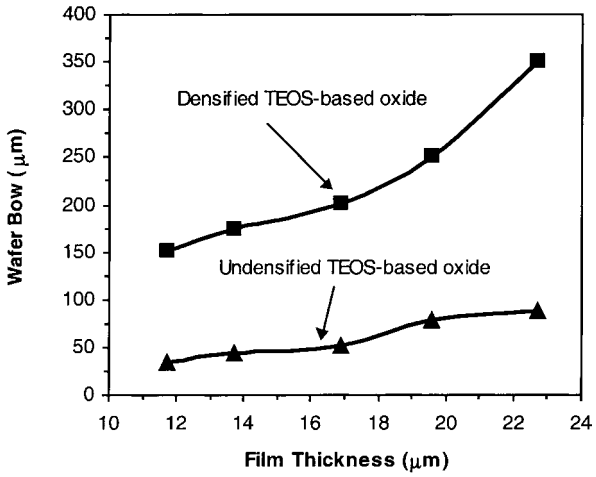


Fig. 7. TEOS-based oxide wafer bow vs. film thickness before and after 1 h densification at 1100°C.

tendency to form cracks is a strong function of film thickness and annealing temperature. Some remarkable failure modes have been observed, examples of which are shown in Fig. 8. Oxide films were annealed at 700°C for 24 h. In Fig. 8(a), 40 μm thick silane-based oxide exhibits surface cracks, which were initiated from the edge, and arrested by the interface. In Fig. 8(b), 25 μm thick TEOS-based film exhibits channeling cracks and a connected channel network was observed, surrounding islands of the intact film. It is well known that film cracking only occurs when the film experiences a tensile stress. Since the thermal expansion coefficient of the oxide is less than that of silicon, tensile stresses will arise when the temperature is raised above the stress-free temperature. In addition, the intrinsic tensile stress generated during temperature ramp up also contributes to the failure of films. Cooling from the deposition temperature, however, leads to compressive stresses in the films and will not result in fracture.

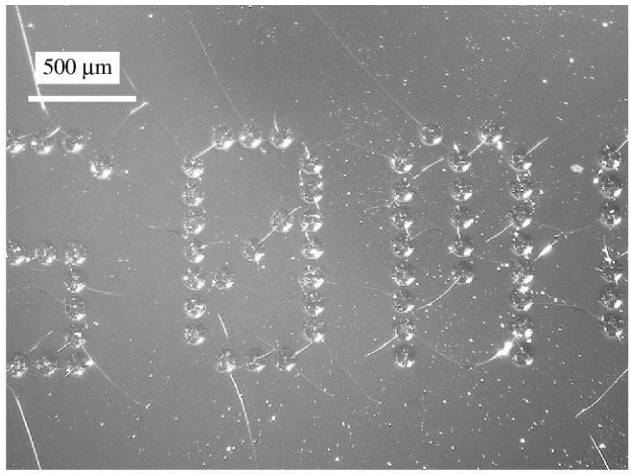
The fracture mechanics of thin films has been analyzed previously. A comprehensive summary was provided by Hutchinson and Suo [12]. The strain energy release rate for a crack propagating in a thin film is given by expressions of the form

$$G = Z\frac{(1-\nu_f)\sigma^2 h_f}{E_f} \tag{3}$$

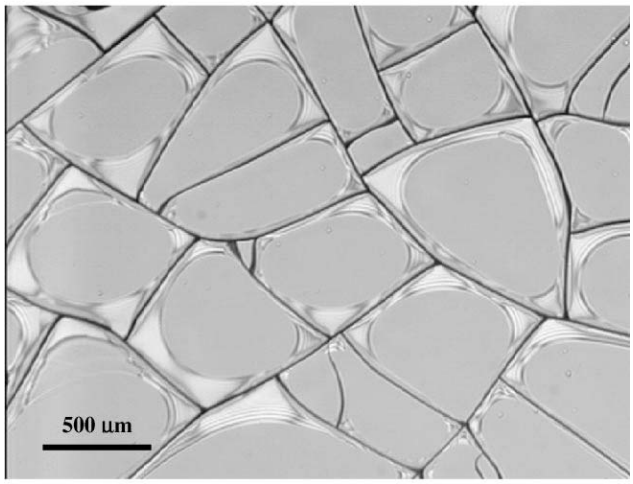
Where h_f, E_f, and ν_f are thickness, Young's modulus, and Poisson's ratio of the film, respectively, and σ is the stress in the film. Z is a dimensionless parameter, which depends on the particular cracking pattern. The two cases of interest for the present work are those of short, microcracks, and long, steady state cracks.

$$Z = \begin{cases} 3.951 & \text{for short, microcracks} \\ 1.976 & \text{for long, steady-state cracks} \end{cases} \tag{4}$$

The crack pattern of silane-based oxide in Fig. 8(a) corresponds to a surface cracks. In this case, Z takes a value of 3.951. On the other hand, for channeling cracks for TEOS-based oxide in Fig. 8(b), Z takes a value of 1.976.



(a)



(b)

Fig. 8. Fracture of oxide films after 24 h annealing at 700°C: (a) 40 μm thick silane-based oxide film; (b) 25 μm thick TEOS-based oxide film.

Fracture occurs when the strain energy release rate exceeds the intrinsic fracture energy of the film material G_c. The critical temperature for fracture can be expressed as a function of film thickness, i.e.

$$T_c = T_0 + \frac{1}{\alpha_s - \alpha_f}\sqrt{\frac{(1-\nu_f)G_c}{ZE_f h_f}} - \frac{\sigma_I(1-\nu_f)}{E_f(\alpha_s - \alpha_f)} \tag{5}$$

where σ_I is the intrinsic stress at given temperature. A complete experimental observation and theoretical calculation for different oxide films is tabulated in Table 2. Notice that using the nominal material properties of oxide the calculated critical temperature to form cracks in TEOS-based oxide (about 950°C) is significantly higher than the observation (about 700°C). This is because the contribution of intrinsic stress was not included for the time being. If the

Table 2
Comparison of predicted and experimentally observed critical cracking temperatures (°C)

Type and thickness	Surface crack equation ($Z = 3.95$)	Surface crack experiment	Channeling crack equation ($Z = 1.976$)	Channeling crack experiment
Silane (10 μm)	1035	<1100	1351	>1100
Silane (20 μm)	812	~800	1036	~1100
Silane (40 μm)	655	~700	813	~800
TEOS (25 μm)	NA	NA	~950	~700
TEOS (25 μm, with 40 MPa intrinsic stress)	NA	NA	~720	~700

effect of intrinsic stress were considered, the critical temperature would be reduced considerably. For example, if the intrinsic stress were assumed to be 40 MPa (this is a reasonable estimation based on the experimental data), the critical temperature would be reduced to 720°C. Moreover, since no detailed material properties and intrinsic stress data are available, the above calculations should be considered representative rather than precise. However, the broad consistency with predictions suggests that it is the tensile residual stress that is primarily responsible for the observed instances of fracture.

In addition, the regions of crack initiation were observed by optical microscopy. An example is shown in Fig. 9. Optical microscopy revealed that many cracks originated from either defects in the film or at the edges of the wafer. This observation can be correlated with the likelihood of there being a higher defect density in the substrate wafer at the edge, which provides sites for crack initiation. This behavior was less pronounced in thinner films, as no cracks were visible macroscopically.

3.3. Engineering solutions

The excessive wafer bows after densification causes difficulties for subsequent processing. From a practical standpoint, the minimum is probably of the most interest. To counteract the compressive stress inherent to the oxide films, several engineering approaches are presented in this section. In our previous study [13], a process called thick buried oxide in silicon (TBOS) was developed. TBOS enables the use of thick oxide films within a multi-stack wafer bonded device by providing localized thick oxide regions with planarized surfaces using chemical mechanical polishing (CMP). This process resulted in reduced wafer bow by at least 50% and eases deep reactive ion etching in the field regions [13].

The second idea is to introduce a second material, such as silicon nitride, with tensile residual stress to counterbalance the effect of the compressive oxide. In order to verify this concept, a sandwich is made by depositing/growing a thin layer of silicon nitride film between the oxide and silicon substrate. As an example, a highly tensile LPCVD nitride film was deposited prior to deposition of the thick TEOS-based oxide film. With proper calculation of thickness ratio and process control, it should be possible to create a wafer with low curvature. The wafer of composite films (0.25 μm LPCVD nitride + 10–25 μm PECVD-TEOS) versus film thickness after 1 h, 1100°C densification is given in Fig. 10. The composite exhibited less and in some case even zero wafer bow for a given film thickness. Further deformation of such composite films was not observed after they were subjected to a 500°C thermal cycling. The stability of the composite films under thermal cycling is illustrated by Fig. 11. Obviously no hysteresis occurred.

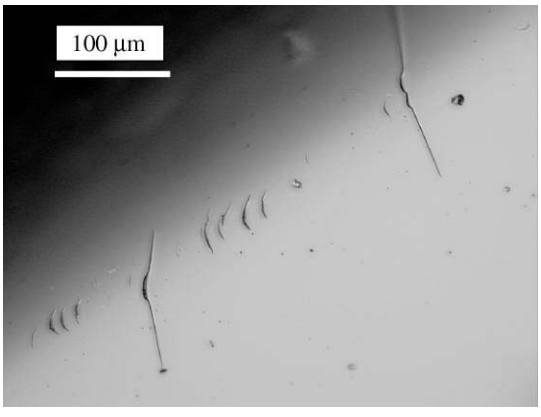


Fig. 9. Cracks at edge of a silane-based oxide film coated wafer.

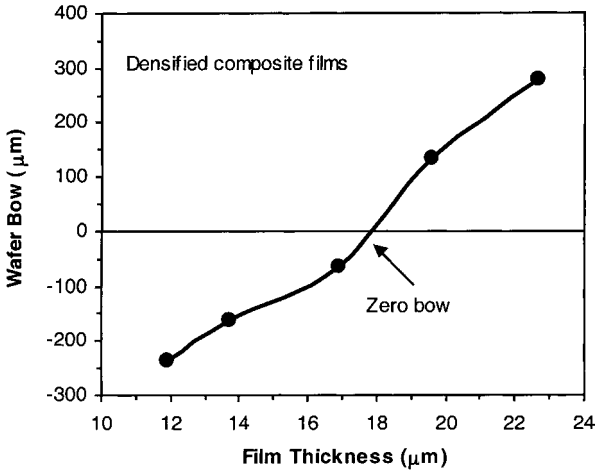


Fig. 10. Wafer bow of composite films (0.25 μm thick LPCVD nitride + 10–25 μm thick PECVD-TEOS) vs. film thickness after 1 h densification at 1100°C.

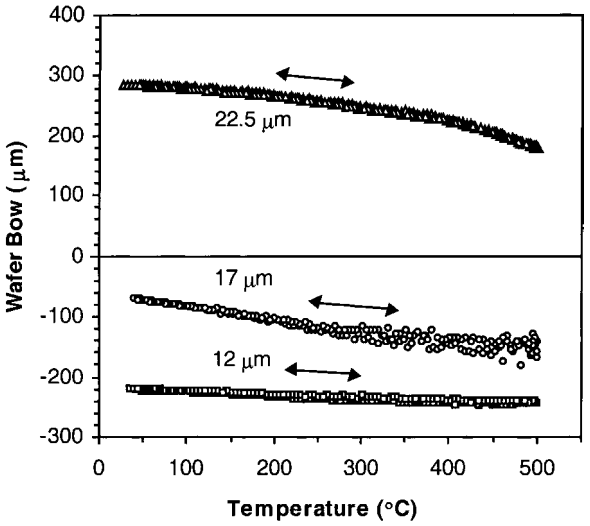


Fig. 11. Stability of wafer bow of 1100°C densified wafers coated with composite films (0.25 μm thick LPCVD nitride + 10–25 μm thick PECVD-TEOS) during a 500°C thermal cycle.

It should be emphasized that, although, there is no deflection macroscopically, the local residual stress was not reduced. As a result, this approach may still encounter problems caused by high residual stress such as delamination. The very high tensile stress (~2500 MPa) is sufficient to cause delamination of the film from the substrate after high temperature annealing. This study only provides a feasible concept in wafer bow control. Parallel efforts to model the stress and strain inside the composite film are underway.

The observation of crack initiation at the wafer edge in Fig. 9 suggests the third idea for crack control. Cracks initiate from the wafer edge because necessary handling during wafer processing leads to inherently poor surface quality. It is feasible to prevent crack propagation from the wafer edge by patterning the oxide to isolate the area of interest from the crack-prone wafer edge. Preliminary experiments revealed that this technique can limit extensive propagation of cracks [14].

4. Conclusions

In this paper, residual stress characterization and fracture analysis of thick silane and TEOS-based PECVD oxide films were conducted in order to understand the controlling mechanism for wafer bow and cracking in thick oxide films and to propose engineering solutions for the design of fabrication processes. Residual stress in oxide films was found to increase considerably upon thermal annealing. Given that the surface analysis of oxide films shows two orders of magnitude difference in hydrogen concentration before and after annealing, it is likely that the hydrogen gases played an important role in governing intrinsic stress. Both thick silane and TEOS-based oxide films were observed to crack after being exposed to the annealing cycle; the tendency to form cracks increased with film thickness and annealing temperature. Mixed mode fracture mechanics was applied to evaluate the critical cracking temperature, and experimental results indicated that the theoretical prediction and test data are highly correlated. Finally, several engineering solutions were proposed and demonstrated to overcome the inherent physical problems associated with wafer bow and film cracks. Most importantly, the proposed engineering solutions not only allowed the specific process integration of a micromotor driven compressor device, but also provide important insights for the design of fabrication processes for other MEMS devices that require high temperature processing of dielectric films.

Acknowledgements

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